Fig. 1 (Prior Art)

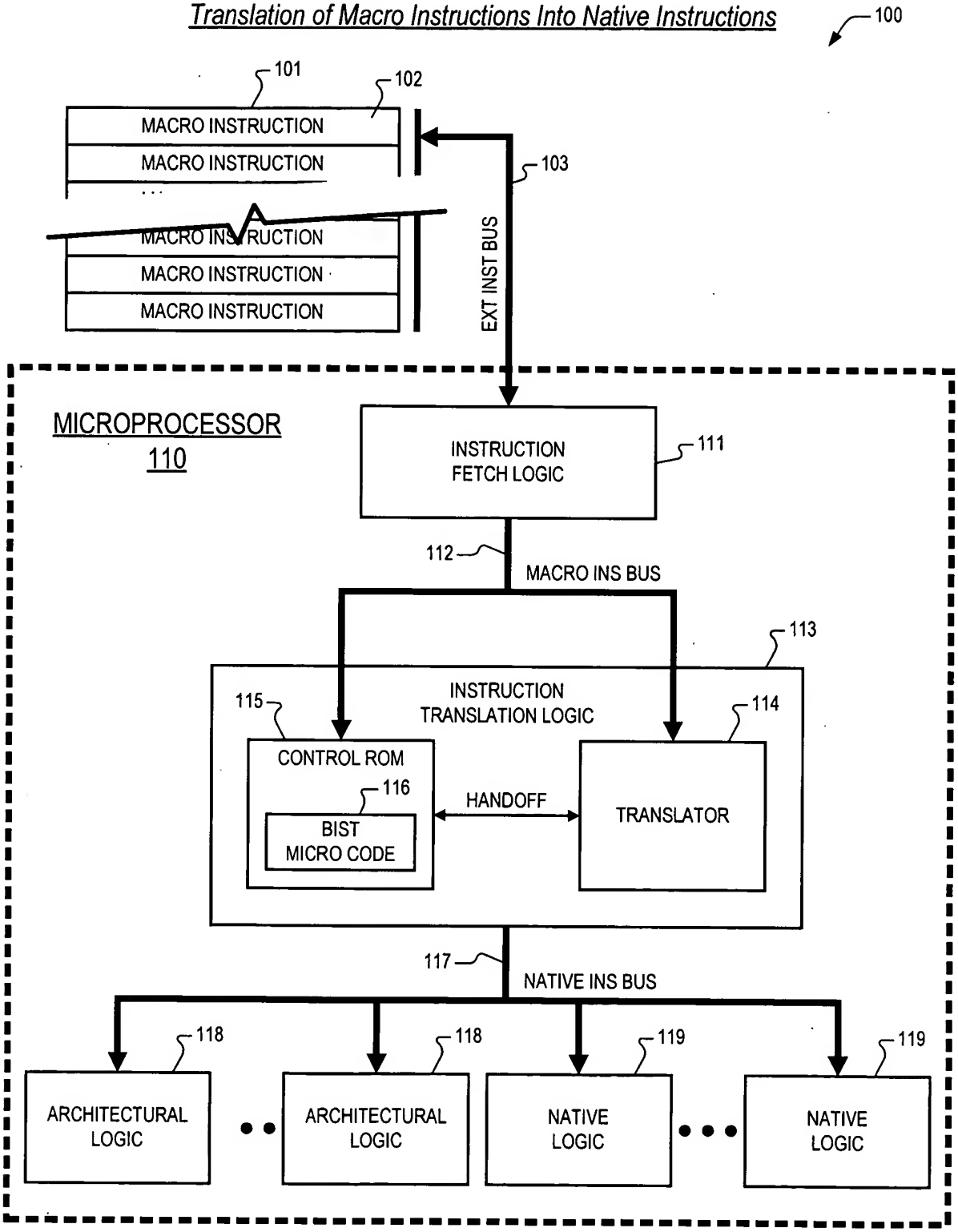


Fig. 2

Indirect Specification of Native Register via Macro Instruction

200

CYCLE	MACRO INS BUS	NATIVE INS BUS
1	ADD [EAX],FFFFFFFFh	+++
2	***	LD NR1,[EAX]
3	***	ADD NR1,NR1,FFFFFFFFh
4	***	ST [EAX],NR1

3 CYCLES

Fig. 3

Translator Bypass for Native Instructions

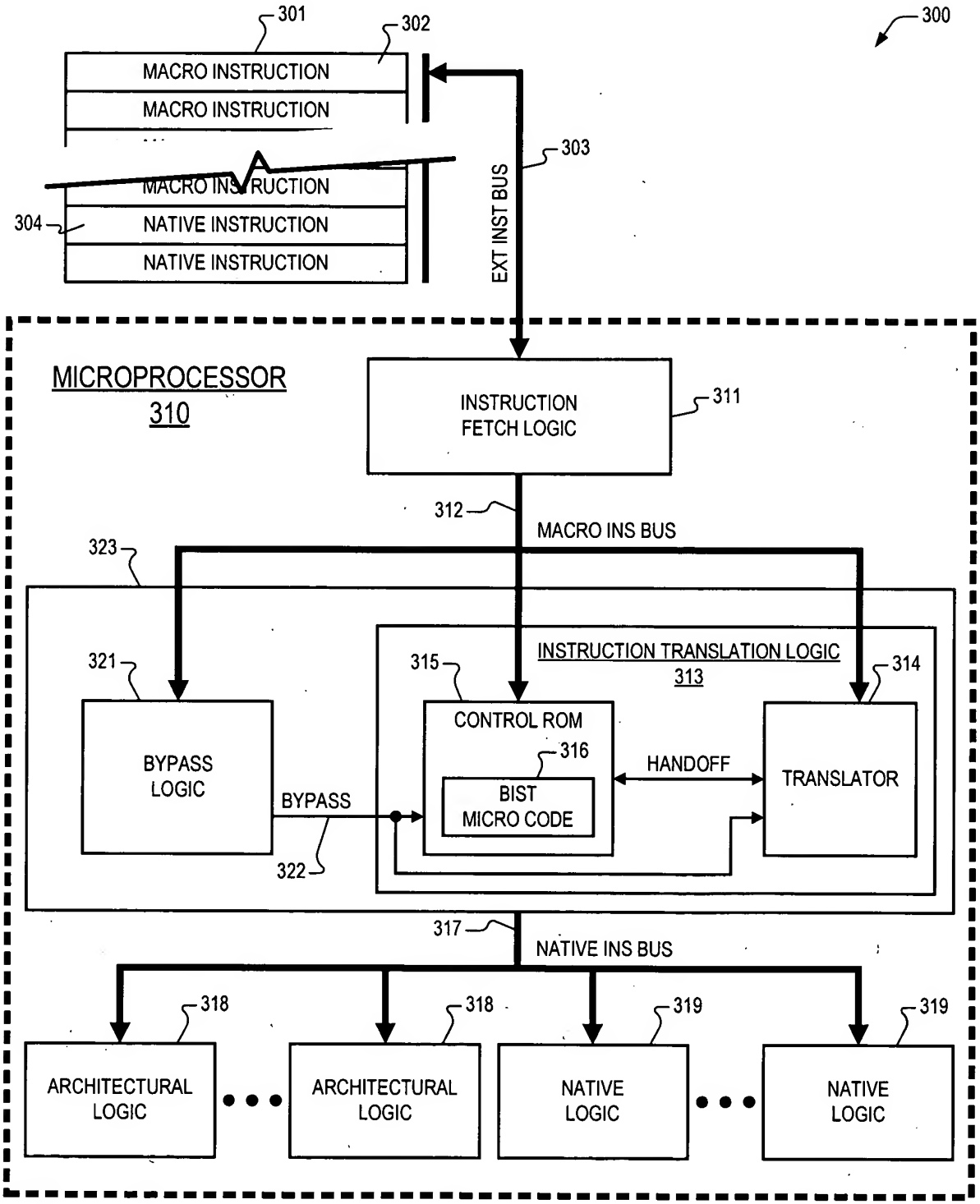


Fig. 4

Translate Stage Logic for Native Instruction Bypass Mode

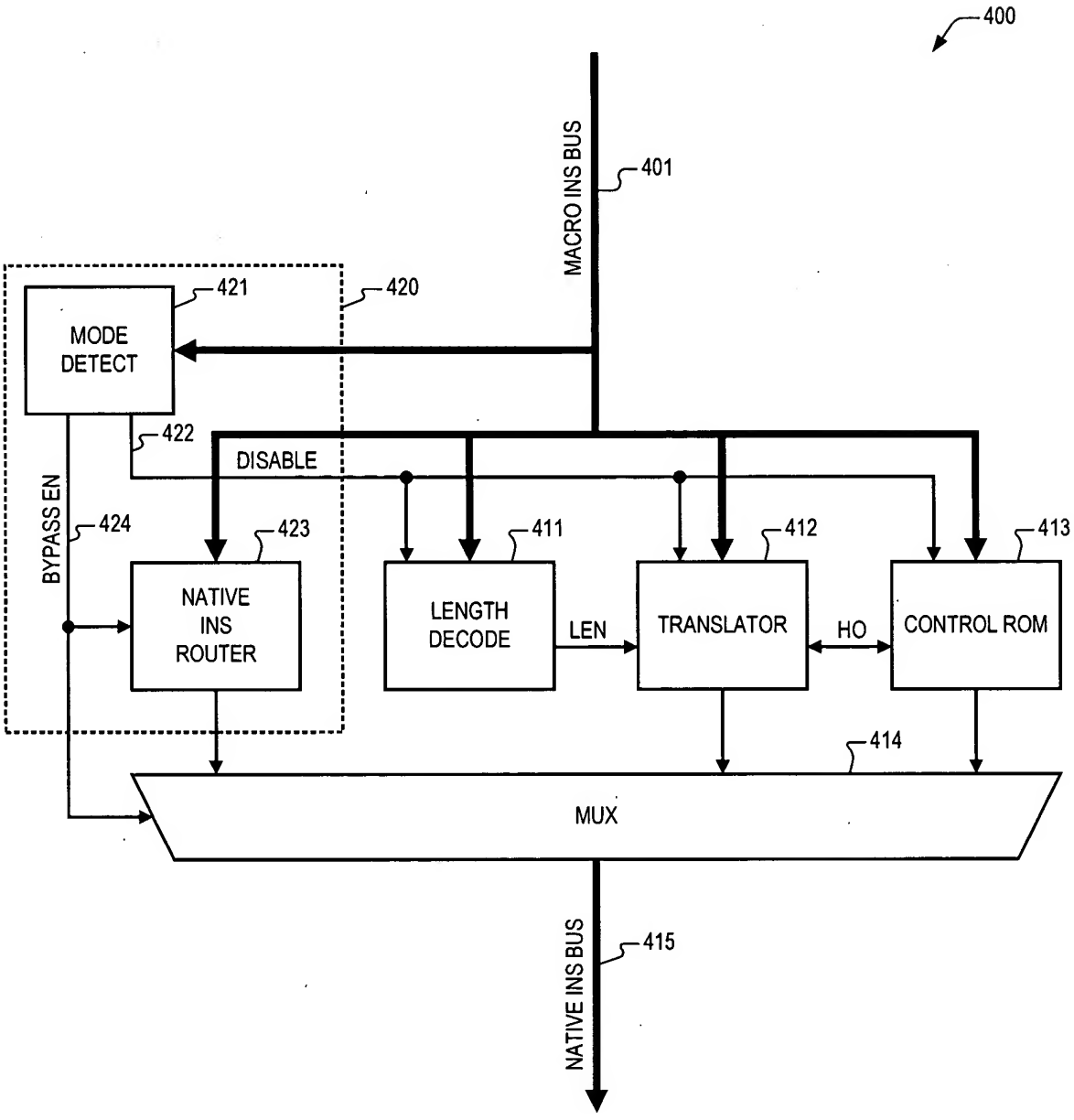


Fig. 5

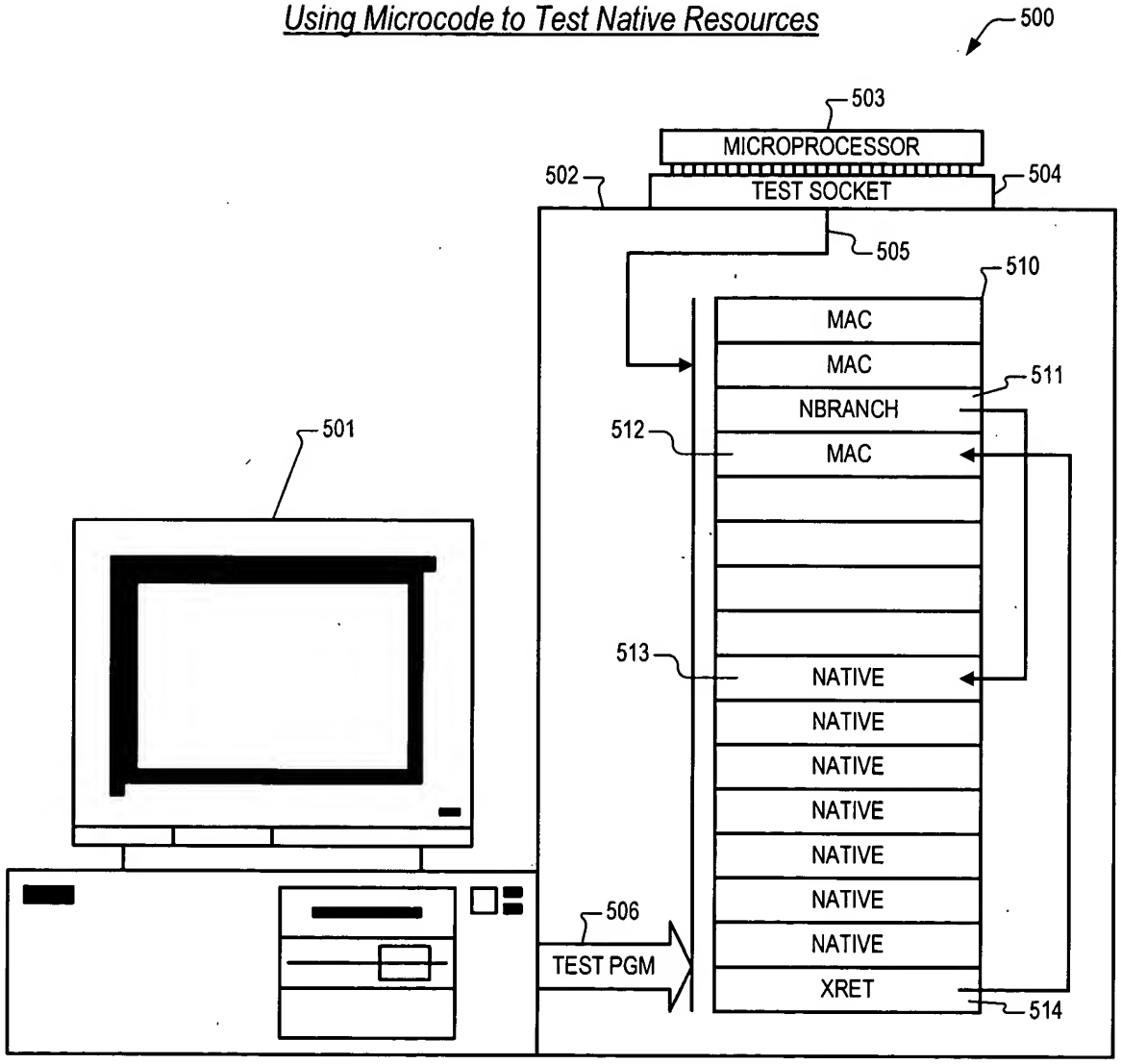
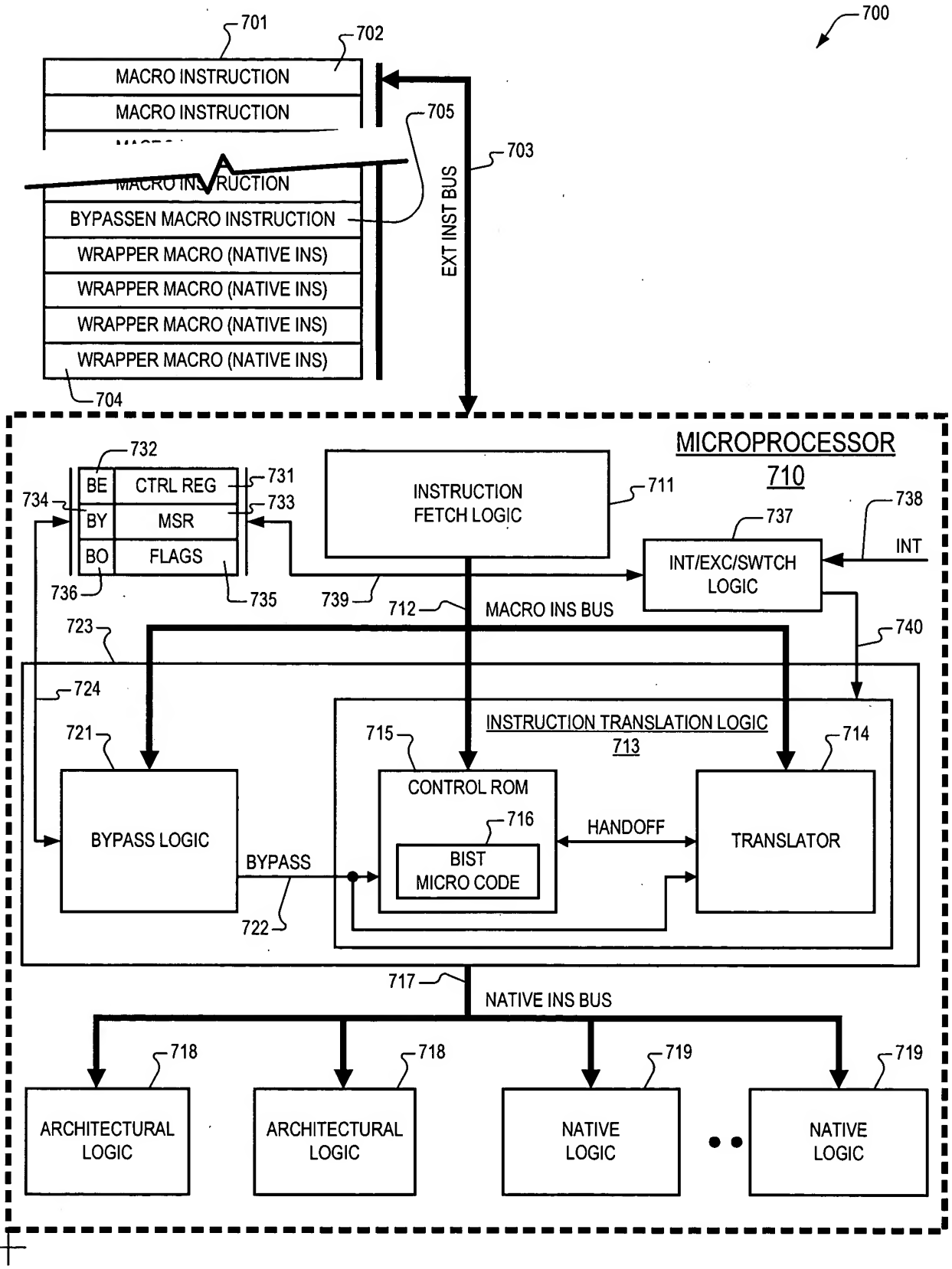

Using Microcode to Test Native Resources
500
503
MICROPROCESSOR
502
TEST SOCKET
504
505
510
MAC
MAC
511
NBRANCH
512
MAC
501
513
NATIVE
NATIVE
NATIVE
NATIVE
NATIVE
NATIVE
NATIVE
506
TEST PGM
XRET
514

Fig. 6

Instruction Sequence for Testing Native Registers 600

CYCLE	MACRO INS BUS	NATIVE INS BUS
1	MOV EAX,*TST1*	+++
2	MOV EBX,*OUTBFR*	LD EAX,*TST1*
3	NBRANCH	LD EBX,*OUTBFR*
4	LD T1,0	JMP [EAX]
5	ST [EBX],T1	LD T1,0
6	NOT T1	ST [EBX],T1
7	ST [EBX],T1	NOT T1
8	***	ST [EBX],T1
9	***	
		+++
1001	XRET	+++
1002	NEXT MAC	JMP [EAX+1]
1003	***	NEXT MAC

Fig. 7


Microprocessor for Executing Native Applications
700
701
702
MACRO INSTRUCTION
MACRO INSTRUCTION
705
703
BYPASSEN MACRO INSTRUCTION
WRAPPER MACRO (NATIVE INS)
WRAPPER MACRO (NATIVE INS)
WRAPPER MACRO (NATIVE INS)
WRAPPER MACRO (NATIVE INS)
EXT INST BUS
704
MICROPROCESSOR
710
732
BE
CTRL REG
731
734
BY
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733
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736
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738
737
INT
INT/EXC/SWTCH
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712
MACRO INS BUS
723
740
724
INSTRUCTION TRANSLATION LOGIC
713
721
715
714
CONTROL ROM
716
HANDOFF
BYPASS LOGIC
BYPASS
BIST
MICRO CODE
TRANSLATOR
722
717
NATIVE INS BUS
718
718
719
719
ARCHITECTURAL
LOGIC
ARCHITECTURAL
LOGIC
NATIVE
LOGIC
NATIVE
LOGIC

Fig. 8

Interrupt-Transparent Native Application Instruction Sequence